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Question Paper Code : X 60461

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Sixth/Seventh Semester
Electronics and Communication Engineering
EC 2354/EC 64/10144 EC 704 – VLSI DESIGN
(Regulations 2008/2010)
(Also common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulations 2009)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Compare CMOS and BiCMOS technology.
2. Draw the DC transfer characteristics of CMOS inverter.
3. List out the limitations of the constant voltage scaling.
4. Draw the small signal model of a MOSFET.
5. State the reasons for the speed advantage of CVSL family.
6. Mention the qualities of an ideal sequencing method.
7. List the basic types of CMOS testing.
8. What is meant by logic verification ?
9. State the operators used in Verilog HDL.
10. Write a Verilog program for a CMOS inverter using switch level modelling.

PART – B **(5×16=80 Marks)**

11. a) i) Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. **(10)**

ii) Draw the CMOS inverter and discuss its DC characteristics. Write the conditions for the different regions of operation. **(6)**

(OR)

b) i) An NMOS transistor has a nominal threshold voltage of 0.16 V. Determine the shift in threshold voltage caused by body effect using the following data. The nMOS transistor is operating at a temperature of 300°K with the following parameters : gate oxide thickness (t_{OX}) = 0.2×10^{-5} cm, relative permittivity of gate oxide (ε_{OX}) = 3.9, relative permittivity of silicon (ε_{Si}) = 11.7, substrate bias voltage = 2.5 V, intrinsic electron concentration (Ni) = $1.5 \times 10^{10}/cm^3$, impurity concentration in substrate (N_A) = $3 \times 10^{16}/cm^3$. Given Boltzmann's constant = 1.38×10^{-23} J/°K, electron charge = 1.6×10^{-19} Coulomb and permittivity of free space = 8.85×10^{-14} F/cm. **(8)**

ii) Explain the principle of SOI technology with neat diagrams. Discuss its advantages and disadvantages. **(8)**

12. a) Derive an expression for the rise time, fall time and propagation delay of a CMOS inverter. **(16)**

(OR)

b) Explain the various ways to minimize the static and dynamic power dissipation. **(16)**

13. a) i) Implement a XOR gate using CMOS logic. **(8)**

ii) Compare CMOS, Dynamic, Domino and Pseudo nMOS logic families. **(8)**

(OR)

b) i) Design a d-latch using transmission gate. **(8)**

ii) Design a 1-bit Dynamic inverting and Non-inverting Register using pass transistor. **(8)**

14. a) Explain the design for testability (DFT) concepts. **(16)**

(OR)

b) Explain the following terms,

i) Silicon debug principles. **(8)**

ii) Boundary scan technique. **(8)**

15. a) Write Verilog HDL code for an 8:3 priority encoder using

i) Casex statement. **(8)**

ii) Data flow modeling. **(8)**

(OR)

b) i) Write Verilog HDL code for an 8-bit ripple carry adder. **(10)**

ii) Briefly describe the difference between inertial delay and Transport delay. **(6)**

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